REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-13 and 19-28 are presently active. Claims 1, 6, 10 and 19 having been amended and Claims 20-28 added by the present Amendment, Claims 14-18 having been previously withdrawn from consideration.

In the outstanding Official Action Claims 1-13 and 19 were rejected under 35 USC 103(a) as being unpatentable over Ohshima et al (U.S. Patent No. 5,019,527) and Havemann (U.S. Patent No. 5,482,894).

In light of the outstanding rejection, Claim 1 has been amended to recite a gate insulating film formed on a second semiconductor region, a first insulating film formed on the gate insulating film, and a second insulating film formed on the first insulating film. Thus, Claim 1 defines a device having a structure in which the first insulating film is sandwiched between the gate insulating film (formed on the second semiconductor region) and the second insulating film.

Ohshima describes a silicon oxide film 12 formed on a second side surface and a top surface but not on a first side surface (e.g. Figure 8). The silicon oxide film 12 is referred to as corresponding to the first insulating film of claim 1.

Havemann describes a conformal dielectric overlayer 42 (e.g. Figure 2D). The conformal dielectric overlayer 42 is formed on a first side surface and with a contact material having a side surface in contact with the conformal dielectric overlayer 42. Further, the conformal dielectric overlayer 42 covers the entirety of a conformal dielectric layer 30. This

conformal dielectric overlayer 42 is referred to as corresponding to the second insulating film of claim 1.

In consideration of the noted elements in the applied prior art, it is noted that Ohshima describes the silicon oxide film 12 (corresponding to the first insulating film) being formed on a second side surface and a top surface but not on a first side surface. Havemann describes the conformal dielectric overlayer 42 being formed on a first side surface and covering the entirety of the conformal dielectric layer 30 (corresponding to the first insulating layer). Hence, the outstanding Office Action states the position that a combination of Ohshima and Havemann renders obvious a device comprising a first insulating film and a second insulating film.

However, the non-volatile semiconductor memory device of Claim 1 comprises a gate insulating film formed on a second semiconductor region, a first insulating film formed on the gate insulating film, and a second insulating film formed on the first insulating film. As explained in more detail below, such a structure is described in neither Ohshima nor Havemann.

In Ohshima, the silicon oxide film 12 is formed on a high concentration impurity region 14, a CVD-SiO_2 film 21 is formed on the silicon oxide film 12, and a resist pattern 22 is formed on the CVD-SiO_2 film 21 (see e.g. Figure 8H). However, the silicon oxide film 12 and the first gate insulating film 3 are not formed as one body, and therefore, the silicon oxide film 12 does not correspond to the gate insulating film of Claim 1. Furthermore, the CVD-SiO_2 film 21 is an interlayer insulating film, and therefore, it does not correspond to the first insulating film of Claim 1. Moreover, the resist pattern 22 does not correspond to the second insulating film of Claim 1.

As shown in Figure 1I of Havemann, the reference discloses a substrate 20 including: (i) a first region in which the substrate 20 is in contact with a contact plug 40; (ii) a second region located next to the first region in which a conductor 26 is formed above the substrate 20 with a gate oxide 22 interposed therebetween; (iii) and a third region located next to the second region in which the conformal dielectric layer 30 is formed above the substrate 20 with the gate oxide 22 interposed therebetween. Further, an organic-containing dielectric layer 32 is formed on the conformal dielectric layer 30. However, the organic-containing dielectric layer 32 is an interlayer insulating film, and therefore, it does not correspond to the second insulating film of Claim 1.

The structure of the non-volatile semiconductor memory device of Claim 1 (wherein a first insulating film is formed between the gate insulating film and the second insulating film) solves the problem in a prior-art device wherein hot carrier becomes trapped in a boundary between the gate insulating film and the second insulating film. This problem is neither recognized, addressed, nor solved by the cited references. Thus, the structure and effect achieved by the claimed invention are not rendered obvious over the teachings of Ohshima and Havemann in the absence of hindsight. Claim 1, as well as the remaining pending claims which recite similar distinguishing features as above discussed, are therefore believed to be patentably distinguishing over the cited art.

Consequently, the present application is believed to be in condition for formal allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)
I:\ATTY\EHK\AMEND-RESPONSES\0039\212706US-AMT.DOC